CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

LISTING OF CLAIMS

No amendments have been made to the Claims. This listing of Claims is presented for the Examiner's convenience.

1. – 2 (Cancelled)

3. (Previously Presented) A power-on reset circuit to generate a reset signal, comprising:

a pull-up resistor connected between a supply voltage and a tracking node;

a pull-down transistor connected between the tracking node and ground potential, the tracking node generating a voltage indicative of the reset signal; and

a voltage divider circuit connected between the supply voltage and ground potential, the voltage divider circuit having a first ratioed voltage node coupled to the gate of the pull-down transistor, wherein the voltage divider circuit comprises:

a first resistor connected between the voltage supply and the first ratioed voltage node;

a second resistor connected between the first ratioed voltage node and a second ratioed voltage node;

a third resistor connected between the second ratioed voltage node and ground potential; and

a shunt transistor connected between the second ratioed voltage node and ground potential, and having a gate responsive to the reset signal.

4. (Original) The circuit of Claim 3, wherein the POR circuit de-asserts the reset signal when the supply voltage reaches a power-up reset level, and asserts the reset signal when the supply voltage falls below a power-down reset level.

5. (Original) The circuit of Claim 4, wherein the power-up reset level comprises a first factor multiplied by a threshold voltage of the pull-down transistor, the first factor determined by the relative resistances of the first and second resistors.

6. (Original) The circuit of Claim 5, wherein the power-down reset level comprises a second factor multiplied by the threshold voltage of the pull-down transistor, the second factor determined by the relative resistances of the first, second, and third resistors.

7. (Original) The circuit of Claim 6, wherein the first and second factors comprise resistance ratios characterized by the voltage divider circuit.

8. (Original) The circuit of Claim 4, wherein the shunt transistor selectively shunts the third resistor in response to the reset signal to provide hysteresis between the power-up reset level and the power-down reset level.

9. (Original) The circuit of Claim 8, wherein the hysteresis between the power-up reset level and the power-down reset level is determined by the third resistor.

10. (Previously Presented) The circuit of Claim 3, wherein the pull-down and shunt transistors comprise NMOS transistors.

11. (Previously Presented) The circuit of Claim 3, further comprising:

a buffer circuit having an input coupled to the tracking node and an output to generate the reset signal.

12. (Original) The circuit of Claim 11, wherein the buffer circuit comprises:

a first inverter having an input coupled to the tracking node, and having an output; and

a second inverter having an input coupled to the output of the first inverter and having an output to generate the reset signal.

13. (Previously Presented) The circuit of Claim 3, wherein the circuit is part of a programmable logic device.

14. (Original) A power-on reset circuit to generate a reset signal, comprising:

a first resistor connected between a voltage supply and a first ratioed voltage node;

a second resistor connected between the first ratioed voltage node and a second ratioed voltage node;

a third resistor connected between the second ratioed voltage node and ground potential;

a pull-up resistor connected between the supply voltage and a tracking node, the tracking node generating a voltage indicative of the reset signal;

a first transistor connected between the tracking node and ground potential, and having a gate coupled to the first ratioed voltage node; and

a second transistor connected between the second ratioed voltage node and ground potential, and having a gate responsive to the reset signal.

15. (Original) The circuit of Claim 14, wherein the POR circuit de-asserts the reset signal when the supply voltage reaches a power-up reset level, and asserts the reset signal when the supply voltage falls below a power-down reset level.

16. (Original) The circuit of Claim 15, wherein the power-up reset level is a predetermined multiple of a threshold voltage of the first transistor, the predetermined multiple determined by a ratio of resistances of the first and second resistors.

17. (Original) The circuit of Claim 15, wherein the power-down reset level is a predetermined multiple of a threshold voltage of the first transistor, the predetermined multiple determined by a ratio of resistances of the first, second, and third resistors.

18. (Original) The circuit of Claim 14, wherein the second transistor selectively shunts the third resistor in response to the reset signal.

19. (Original) The circuit of Claim 14, wherein the first and second transistors comprise NMOS transistors.

20. (Original) The circuit of Claim 14, further comprising:

a buffer circuit having an input coupled to the tracking node and an output to generate the reset signal.

21. (Original) The circuit of Claim 20, wherein the buffer circuit comprises:

a first inverter having an input coupled to the tracking node, and having an output; and

a second inverter having an input coupled to the output of the first inverter and having an output to generate the reset signal.

22. (Original) The circuit of Claim 14, wherein the POR circuit is part of a programmable logic device.

23. – 24. (Cancelled)

25. (Previously Presented) A power-on reset circuit to generate a reset signal, comprising:

a pull-up resistor connected between a supply voltage and a tracking node;

a pull-down transistor connected between the tracking node and ground potential, and having a gate responsive to a control voltage;

means for generating the control voltage as a predetermined factor of a threshold voltage of the pull-down transistor; and

means for selectively adjusting the predetermined factor in response to the reset signal.

26. (Previously Presented) A power-on reset circuit to generate a reset signal, comprising:

a pull-up resistor connected between a supply voltage and a tracking node;

a pull-down transistor connected between the tracking node and ground potential, and having a gate responsive to a control voltage;

means for selectively adjusting the predetermined factor in response to the reset signal; and

means for generating the control voltage as a predetermined factor of a threshold voltage of the pull-down transistor, wherein the means for generating comprises:

a first resistor connected between the voltage supply and a first ratioed voltage node;

a second resistor connected between the first ratioed voltage node and a second ratioed voltage node; and

a third resistor connected between the second ratioed voltage node and ground potential.

27. (Original) The circuit of Claim 26, wherein the means for selectively adjusting comprises a shunt transistor connected in parallel with the third resistor and having a gate responsive to the reset signal.

28. (Cancelled)

29. (Previously Presented) The method of Claim 30, wherein the control voltage comprises a predetermined fraction of the supply voltage.

30. (Previously Presented) A method for generating a reset signal, comprising:

providing a pull-up resistor connected between a supply voltage and a tracking node;

providing a pull-down transistor connected between the tracking node and ground potential;

generating a control voltage using a voltage divider circuit; and

controlling the conductivity of the pull-down transistor with the control voltage; and

selectively adjusting the predetermined fraction in response to the reset signal.